HH38WX-ST THEORY OF OPERATION

A. PLL, the Phase-Locked-Loop frequency synthesizer

See Frequency synthesizer block diagram and schematic.

1. Introduction

The synthesizer consists of the following.
Components: PLL IC (IC301)
CRYSTAL (X301)
VARICAP DIODE (D10)
TRANSISTOR (Q15, Q16, Q3, Q17, Q18)
LCD DISPLAY (LCD1)

IC301 is a CMOS LSI that includes most of the PLL block.
The VCO with varicap-diode D10 as part of the tank circuit.
Q3 is a switching transistor to connect or disconnect the tuning capacitor in the VCO oscillator tank circuit for transmitter or receiver.

2. Reference Frequency

The crystal X301 (4.5 MHz) and other components at pin 1 and pin 80 of IC301 form a clock frequency oscillator. The oscillator output is internally fed to a divide-by-1800 to produce a 2.5 kHz signal. That is the reference input for the phase detector.

3. VCO, the voltage-controlled-oscillator

Q17 is the oscillator with the varicap-diode D10 as part of the tank circuit. With the control voltage applied to D10, the VCO oscillates over the required range of 13.4825 MHz to 16.710 MHz.

4. Programmable Divider and its Control Function

The programmable inputs for each channel are set inside IC 301. The input signal of IC 301 is obtained by the key matrix which is formed by T1 (pin 30) to T4 (pin 27) and K10 (pin 35) to K13 (pin32). For any key matrix input, the internal code generator provides an appropriate binary control data for the programmable divider of that channel frequency. Since the binary data is necessary to change under transmit mode and receive mode, one additional bit is required at pin 3 of IC 301 to allow the ROM to recognize the mode is Tx or Rx. During transmit the tact switch makes Q304 base grounded by transistor Q306. The PLL IC works under transmit mode. The programmable divider output is fed to the phase detector for comparison with the 2.5 kHz reference frequency.

5. Phase Detector and VCO Control

The phase detector is a digital phase comparator which compares the leading edge of the reference frequency with the programmable divider output square wave and produces a series of pulses whose DC level depends on whether the phase error is leading or lagging. The phase detector output (pin 78 of IC301) is fed to a charge pump and then fed to pin 78 of IC301. The low pass filter output at pin 78 of IC301 is filtered and fed to varicap diode D10 to control the VCO frequency. The result is that the second order component of the PLL frequency and the loop dynamic characteristics are essentially controlled by the active low pass filter.

6. TRANSMIT/ RECEIVE Buffer Amplifier

The VCO output is fed to the buffer transistor Q18, from the secondary tap of IFT coil L7.

7. Transmit Frequency Doubler

The output of Q17 is obtained at its emitter and is fed to the base of transistor Q28, which is a

frequency doubler. The output frequency of Q28 is doubled in relation to its input frequency. The output tank circuit of Q28 is a double-tuned circuit (27 MHz). It is consisted of L11 and L12, in order to stop the fundamental frequency 13.5 MHz.

8. Switching of Tuning Capacitor in VCO oscillator tank circuit

The VCO circuit must be tuned in a wide range of frequencies.
In Receive mode, Q3 is Off, thus C66 is open. The VCO tuning circuit is consisted of L10, C63, C64, C65, C67 and the varicap diode D10. It operates in the frequency range of 16.270 MHz to 16.710 MHz.
In Transmit mode, Q3 is On, thus C66 is added in parallel to L10. The frequency range is then step down to 13.4825 MHz – 13.7025 MHz.

9. Fault Protection

IC301 included a phase detector which functions as a lock detector. If the frequency lock is lost, then pin 11 becomes low and the base of Q33 is cut off, to prohibit transmission. Transmission cannot be made if a code other then those for 40 channel is input to IC301.

10. Frequency Stability

Let: F0 = Crystal Oscillator Frequency
FR = Phase Detector Reference Frequency
FVCO = VCO Frequency
FT = Transmit Frequency
Then = FR = F0/1800, and under locked conditions:

$$FR = \frac{FVCO}{N}$$

Where N is the programmable divider dividing ratio

From which it can be seen that the percentage error in FT is the same as the percentage error in F0. The stability of the crystal oscillator is determined primarily by the crystal and to a lesser extent by the active and passive components of the oscillator. The choice of crystal and components is such that the required frequency stability is maintained within the required voltage and temperature range.

B. Tx, Transmitter Section

1. RF Amplification

The output of the frequency doublee Q28 is fed through double-tuned coils (27 MHz) L11, L12 to the base of Tx pre-amplifier Q33. The output is then passed through the tuning circuit L13 to Tx driver Q29. The Q29 output is coupling through L14 and C95 to the base of final Tx amplifier Q30. Finally, the output of Q30 is supplied to the antenna through L-C tuning circuit.

2. Circuit for Suppression of Spurious Radiation

The tuning circuit between the frequency synthesizer and the Tx pre-amplifier Q33, plus the 3-section "PI"-type band pass filtering network: C99, C100, C102, C105, C103, C106, C104 in the Q30 output circuit, served to suppress spurious radiation. The filtering network also works as the impedance matching network between Q30 and the antenna.

3. Circuit for Power Limiting

After finished all alignment, the constant voltage supply circuit limits the available power to 4W. The VR5 and transistors Q26, Q27, Q32 control the supply voltage of Tx amplifier and other RF meter. Tune all the trimming parts for maximum indication of Tx power meter and adjust VR7 for 4.0 W indication of Tx meter.

4. Modulation

The microphone input is sent to the audio power amplifier IC3, then fed to the modulation transformer T1. The audio output at the secondary of T1 is fed in series with the B+ supply voltage to the collectors of Tx driver Q29 and Tx final Q30. Thus achieves the collector modulation for these two stages.

5. Circuit for Modulation Limiting

A portion of the modulating voltage is rectified by D11 then turns on Q24, Q25. Which attenuate the microphone input to mic amplifier IC3. The resulting feedback loop keeps the modulation from exceeding 95 percent when the input signal is increased 40 dB above the original level required to produce a 50 percent modulation.

C. Rx, CB Receiver Section, 40 channels

The CB receiver is a double conversion superheterodyne with the first IF at 10.695MHz and the second IF at 455kHz. The synthesizer supplies the first local oscillator 10.695MHz below the received frequency and the second local oscillator at 10.240MHz. The detector output provides reverse AGC to the previous stages of Q10 and Q12. The AGC voltage is also amplified by Q13 and used to drive the RF attenuator D5.

D. Wx, Weather Band Receiver Section, 10 channels

The Weather receiver is a dual conversion super-heterodyne type with the first IF 10.695 MHz and the second IF 455 kHz. The PLL synthesizer supplies the local oscillation frequencies at 10.695 MHz below the RF frequency to produce a first IF signal of 10.695MHz. Q7 amplifies the incoming weather signals. Q8 mixes the incoming weather signal and the local oscillator signal to generate the IF frequency possessing audio information. The 455KHz amplifier circuit inside IC1 amplifies the 455KHz signal to make enough level for discriminating the audio signal. IFT L9 and R41 are working as a FM detector.

E. Compander circuit

IC201 TA31101F is the Compander which acts for compressing the dynamic range of the audio signal in the transmitting path, and expanding the dynamic range of the audio signal in the receiving path. This will result in an improved signal to noise ratio.